

10th International Symposium on Electrochemical Impedance Analysis 2014

Electrochemical Impedance Spectroscopy of n-Si(100) Pre-etched by KOH or BHF

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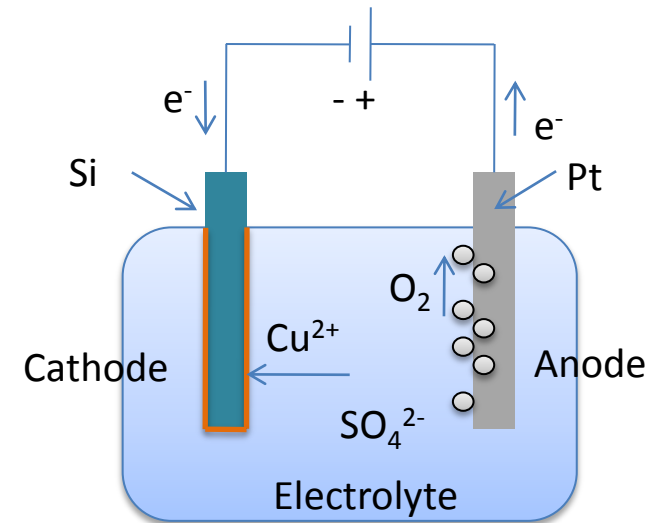
Content

- Motivation and Seedless Electroplating Basic Principles
- Previous Investigations: CV and Selective Deposition
- EIS Research Topics
- Equivalent Circuits
- Results and Discussions
- Summary

Motivation and Basic Principles

Motivation and Basic Principles

- Better understanding of Si seedless electroplating
 - create microstructures
 - improve models
- Further development of new applications in electroplating:
 - solar cells ^[1]
 - fuel cells ^[2]
 - IC technology ^[3]
 - MEMS



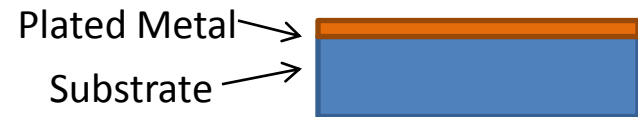
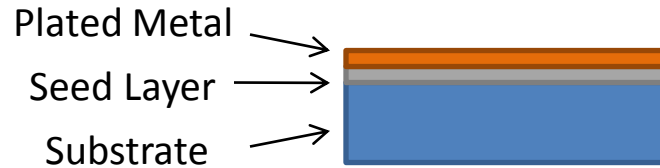
[1] S.W.Glunz, *Advances in OptoElectronics*, Article ID 97370, (2007)

[2] M.Hayase et al, *PowerMEMS 2005*, Japan, p. 128

[3] A.Uhlig, Atotech Deutschland GmbH, "Electroplating aspects in 3D IC Technology", Sematech Workshop San Diego, USA, 2008

Basic Principles

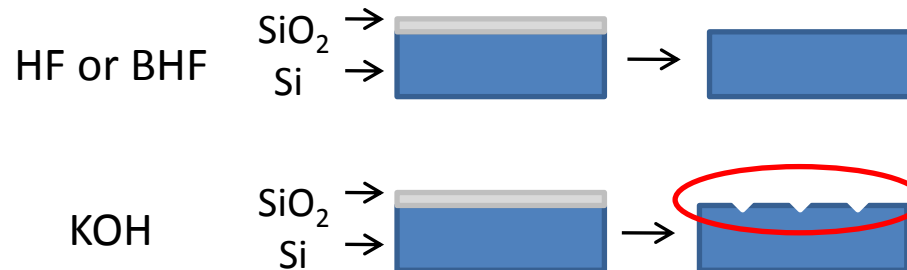
Seed layer X Seedless



- High adhesion
- Homogeneous plating
- Well developed processes

- Low adhesion
- Inhomogeneous plating
- Less machines and process steps
- Different (new) applications

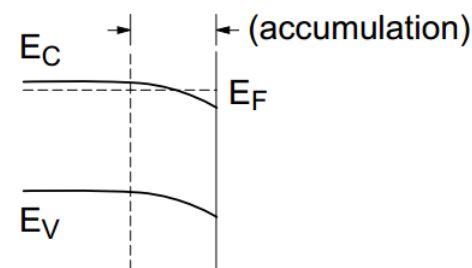
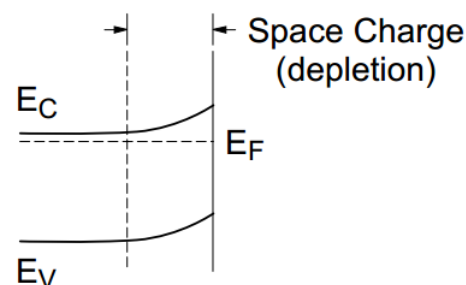
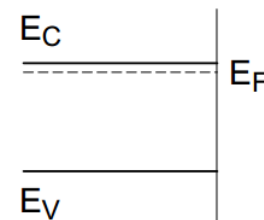
- Etching Processes (SiO_2 removal):



Basic Principles

Semiconductor/Electrolyte Interface

- Flat band ($E = E_{fb}$)
 - no current flowing through the interface
- Depletion regime ($E > E_{fb}$)
 - HF: WE as anode
 - H_2SO_4 : current blocked (dark)
- Accumulation regime ($E < E_{fb}$)
 - WE as cathode



Electrode Solution [4]

[4] A. W. Bott, *Current Separations*, **17:3**, 87 (1998)

Previous Investigations

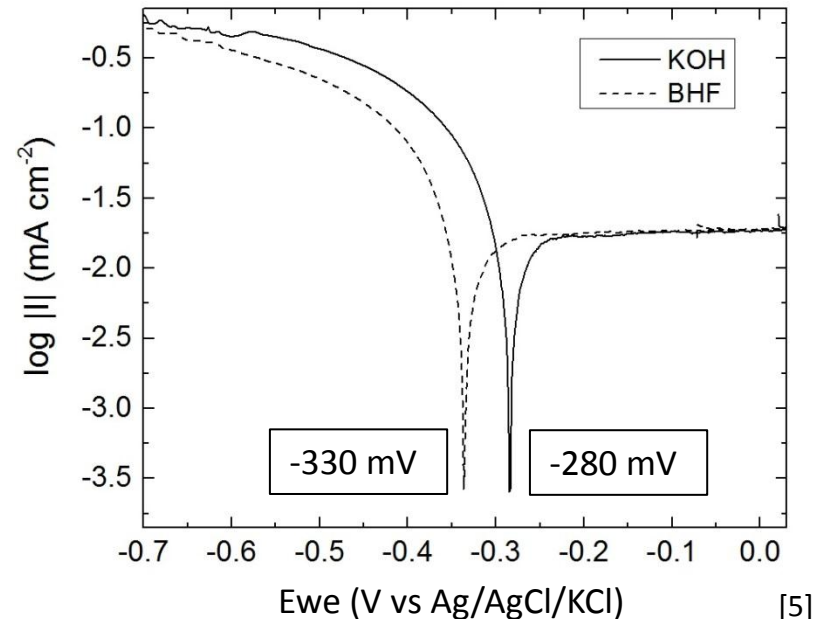
Previous Investigations

- CV n-Si(100)

BHF- vs KOH-etched

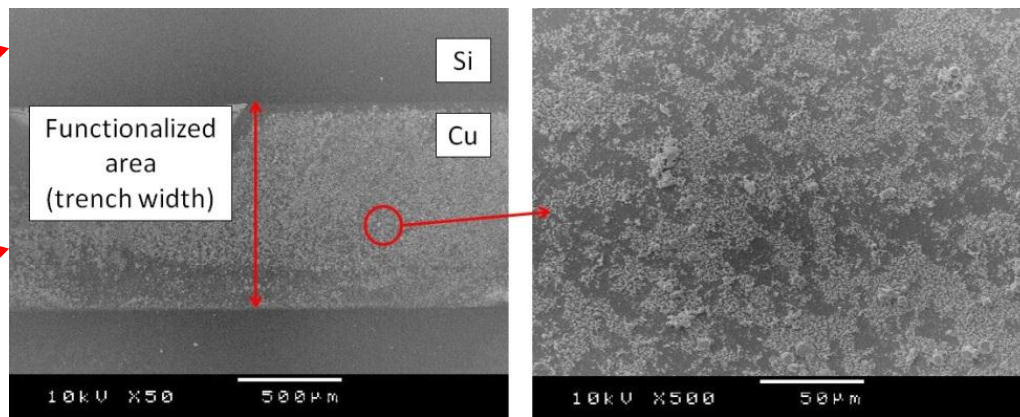
- n-type 5 - 10 Ohm cm
- 0.01 M CuSO_4 + 0.05 M H_2SO_4

- Selective electrodeposition



EIS: BHF
etched area

EIS: KOH
etched area



[5] F.G.C. Lima, U. Mescheder and H. Reinecke, "Electroanalyses of Silicon Surfaces for Seedless Electroplating", 6th ElecNano, Paris, 2014

[6] F.G.C. Lima, U. Mescheder and H. Reinecke, "Maskless Selective Electrodeposition on Silicon", 65th Annual Meeting of ISE, Lausanne, 2014

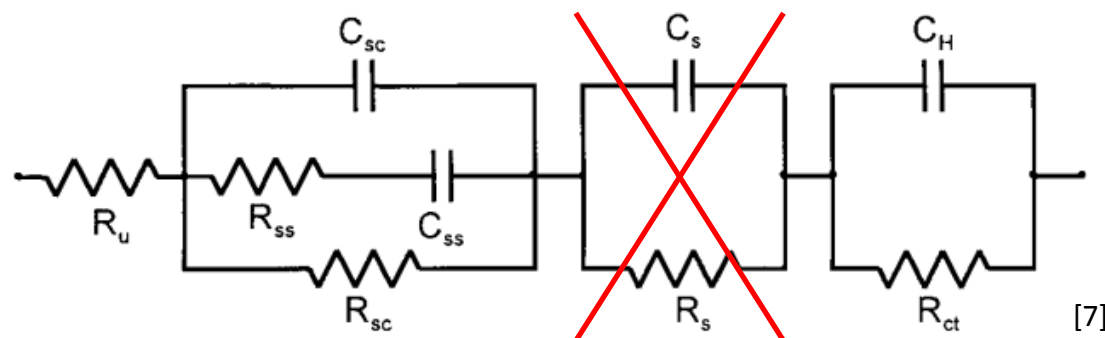
Research Topics

Research Topics

- Understand effects of seedless electroplating on rough surfaces in comparison to quasi-perfect planes
- Electrochemical impedance spectroscopy (EIS) used to investigate changes of the following:
 - Helmholtz layer
 - space charge layer
 - surface states

Equivalent Circuit

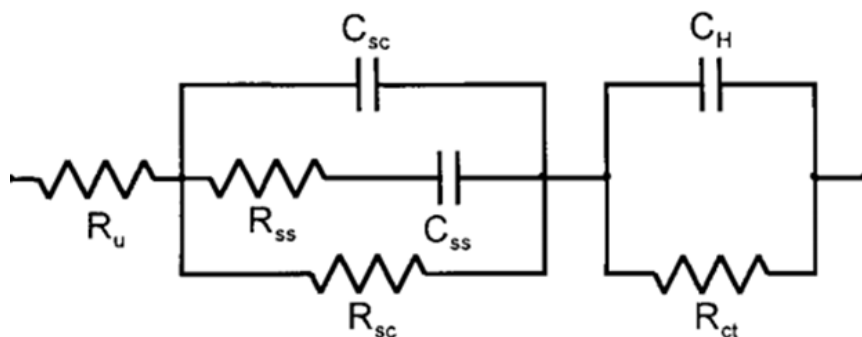
Equivalent Circuit



R_u : substrate and electrolyte resistance
 C_{sc} : space charge capacitance
 R_{sc} : space charge resistance
 C_{ss} : surface state capacitance
 R_{ss} : surface state resistance
 C_s : oxide capacitance
 R_s : oxide charge resistance
 C_H : Helmholtz Layer capacitance
 R_{ct} : charge transfer resistance

- Oxide removed prior to EIS

- C_s and R_s can be excluded [8]



[7] V. Lehmann, "Electrochemistry of Silicon: Instrumentation, Science, Materials and Applications", Wiley-VCH Verlag GmbH, Amsterdam, 2002.

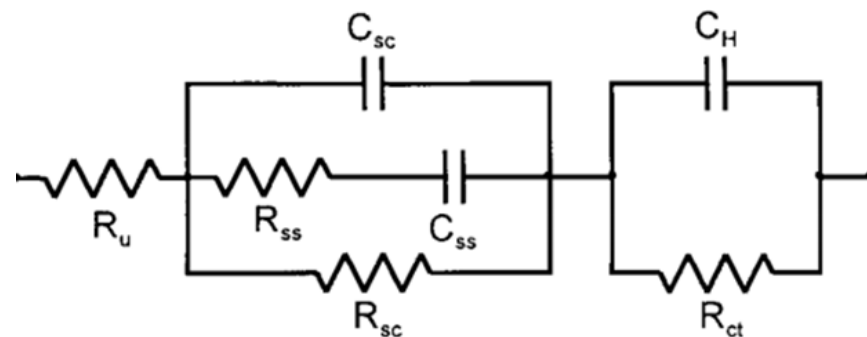
[8] P. Schmuki, H. Böhni and J. A. Bardwell, *J. Electrochem. Soc.*, **142**, 1705 (1995)

Equivalent Circuit

- Depletion Regime

- $C_{sc} \ll C_H$ [8]

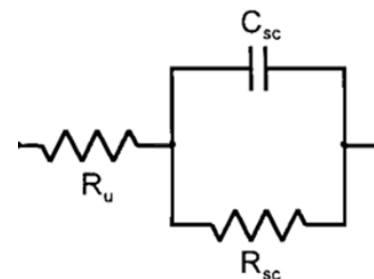
Helmholtz layer capacitance (C_H)
can be neglected



- Monocrystalline Si(100)

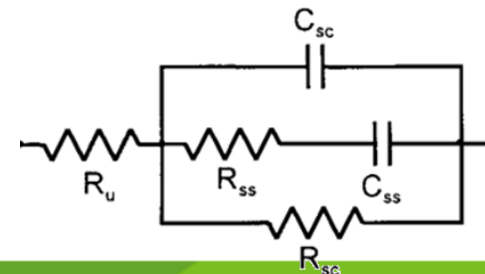
- BHF etched:

surface states (SS) neglected



- KOH etched:

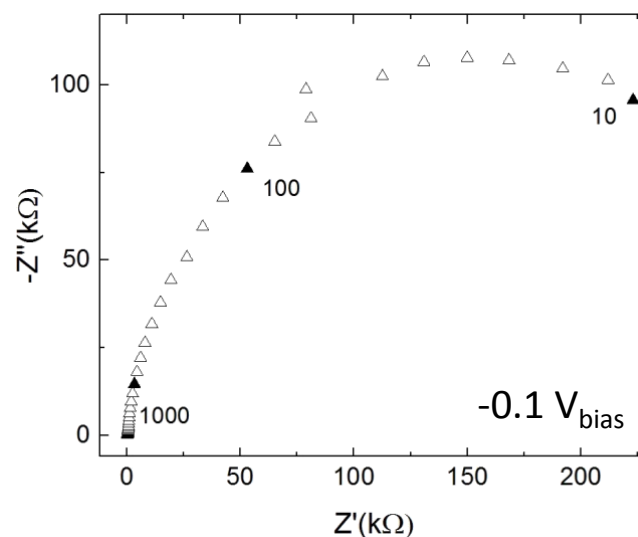
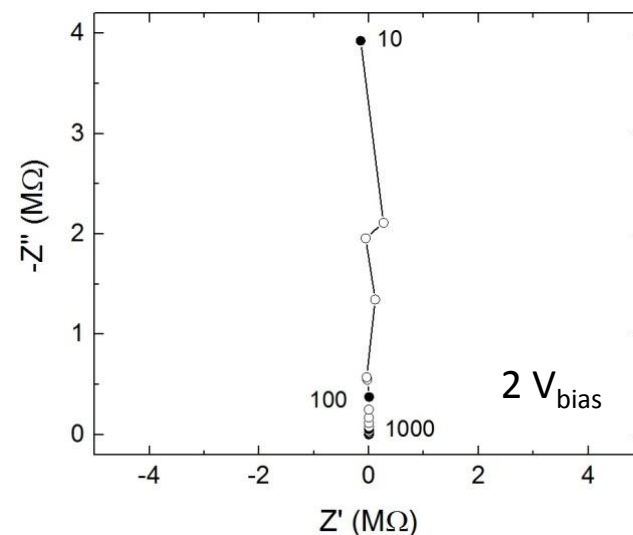
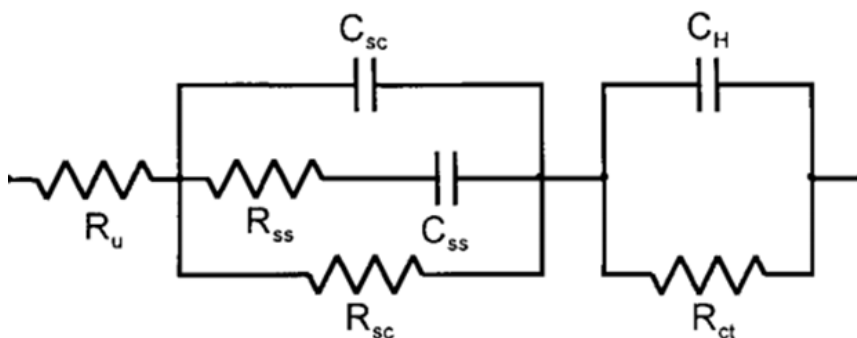
SS should increase (due to surface defects)



[8] P. Schmuki, H. Böhni and J. A. Bardwell, *J. Electrochem. Soc.*, **142**, 1705 (1995)

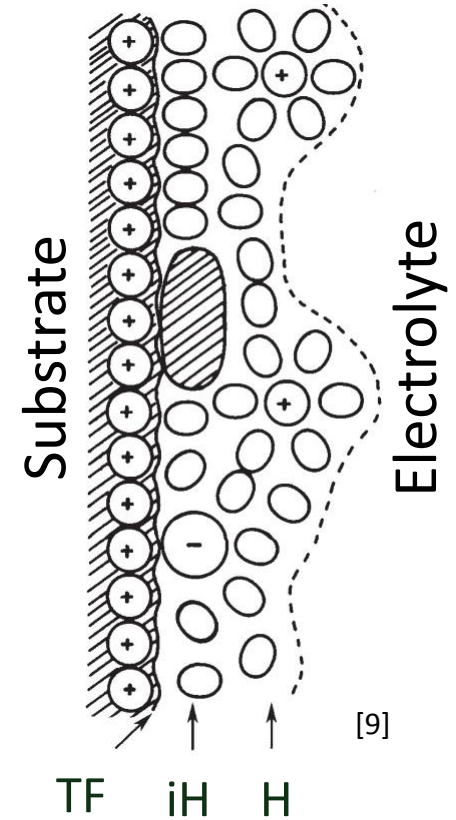
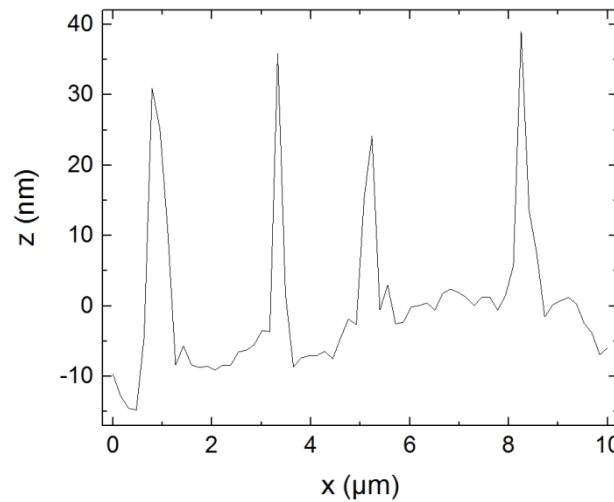
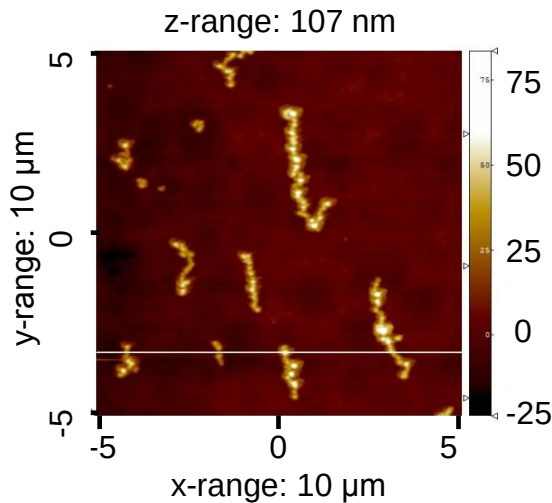
Results and Discussion

- Space Charge
 - Depletion regime
 - Anodic current flowing
 - Accumulation regime
 - Cathodic current flowing



Results and Discussion

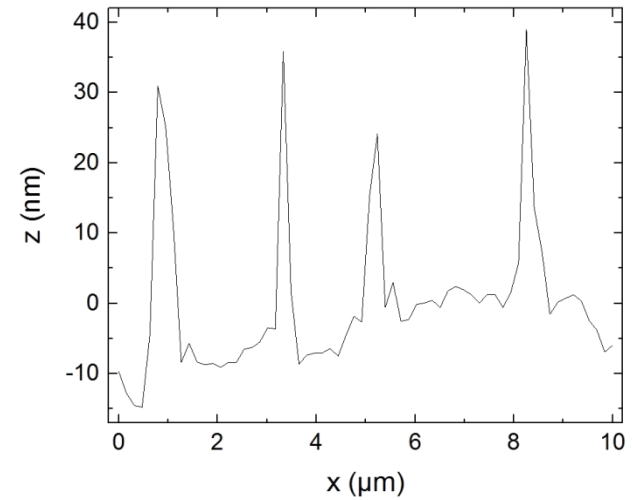
- Helmholtz layer capacitance if etched by
 - BHF: flat capacitor
 - KOH: rough capacitor plate
 - C increases proportionally to A



[9] W. Plieth, "Electrochemistry for Material Science", Elsevier, Amsterdam, 2008

Results and Discussion

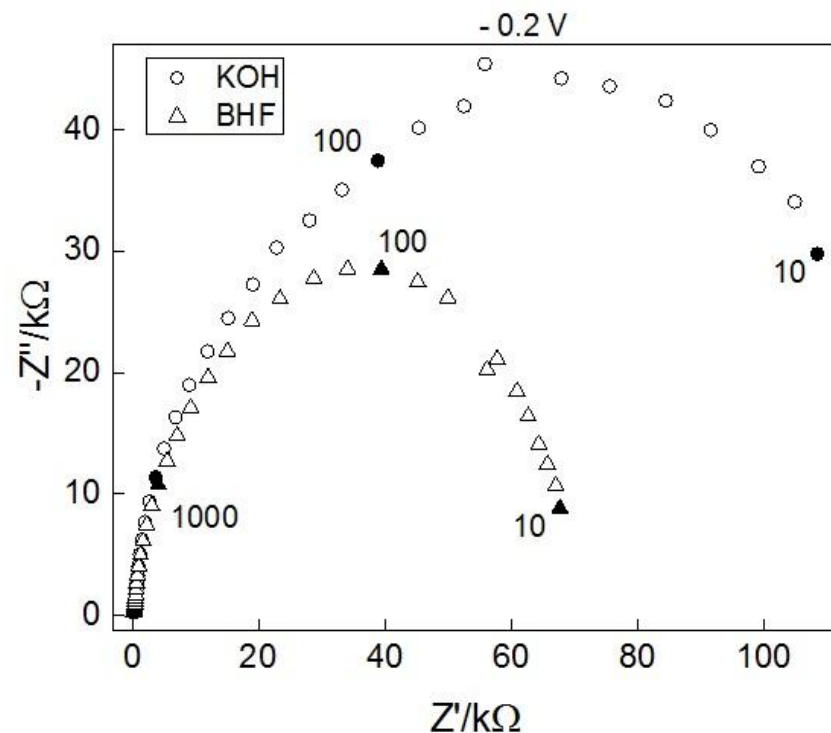
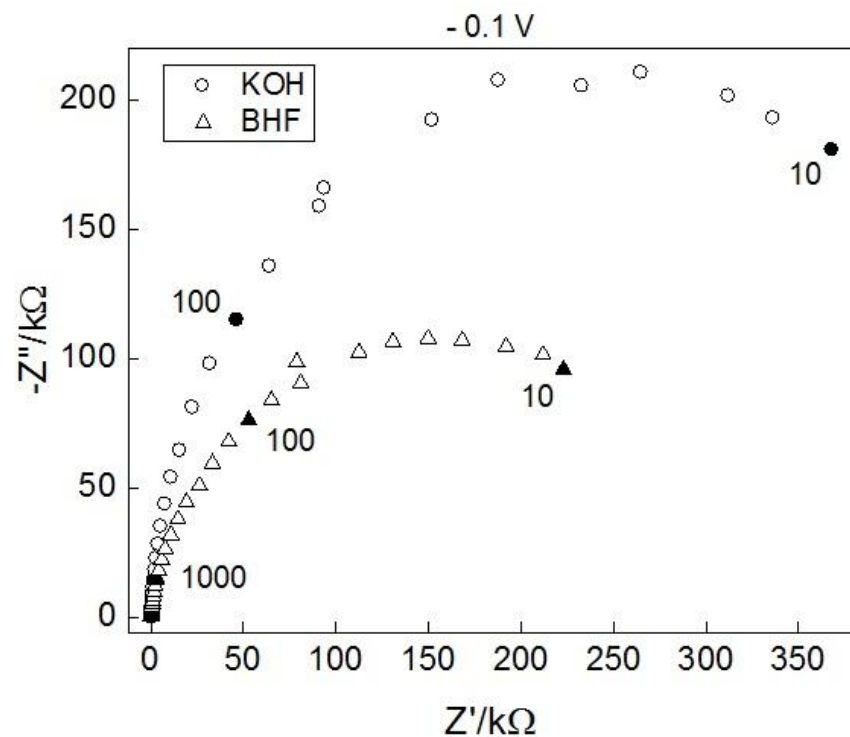
- Space charge capacitance
 - $d = 0.01$ to $1 \mu\text{m}$ [4,8]
 - KOH-etched:
 - A increases
 - Assume d (morphology dependent) keeps constant
 - C_{sc} increases less in magnitude compared to C_H
 - RC equivalent circuit is not appropriated anymore
 - C_{total} decreases in comparison to BHF-etched samples
- Surface states: expected to increase (KOH-etched)
 - Small magnitude in comparison with C_{sc}



[4] A. W. Bott, *Current Separations*, **17:3**, 87 (1998)

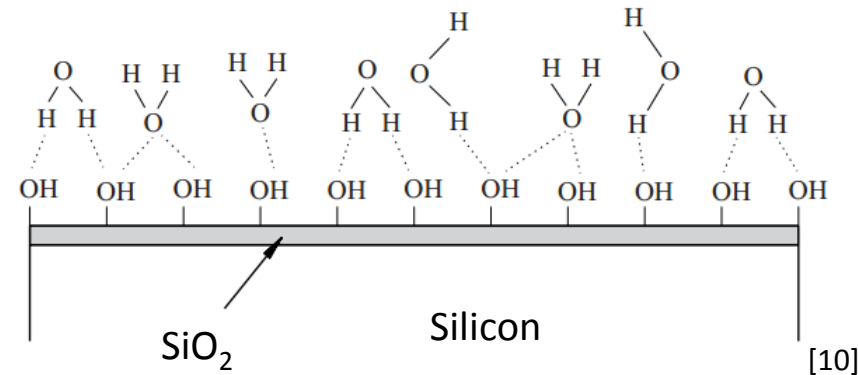
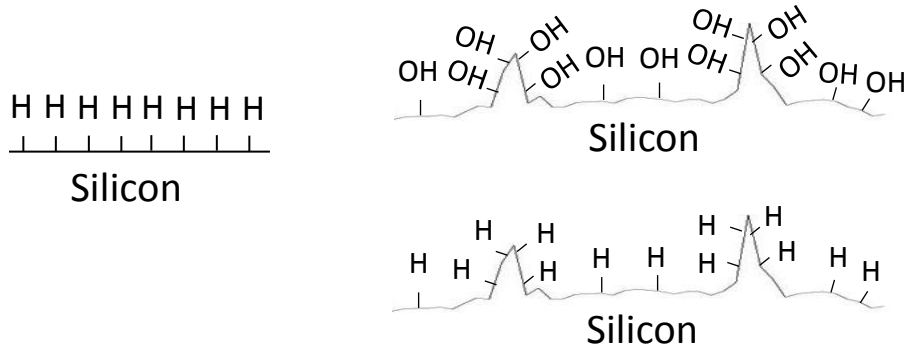
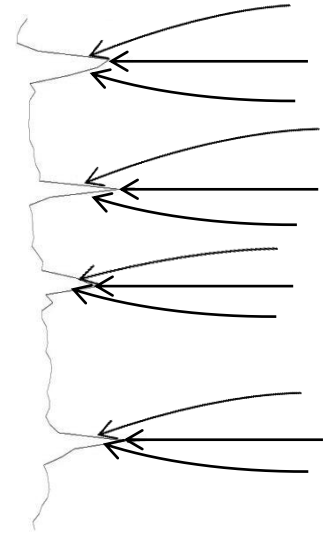
[8] P. Schmuki, H. Böhni and J. A. Bardwell, *J. Electrochem. Soc.*, **142**, 1705 (1995)

Results and Discussion



Results and Discussion

- KOH-etched: higher resistance
 - Few possible explanations:
 - Current concentration due smaller conductive area
 - OH terminations more stable than the H-terminations after BHF etching
 - After cleaning process, probably H-termination
 - more stable H-terminations than BHF-etched



[10] M. Wiegand, "Auswirkungen einer Plasmabehandlung auf die Eigenschaften des Niedertemperatur-Waferbondens monokristalliner Siliziumoberflächen", Doctor Thesis, Germany, 2001.

Summary

Summary

- C_{total} decreases (compared with BHF-etched) when etching samples by KOH
 - C_{SC} (morphology depend) assumed to increase (less in magnitude than C_{H})
 - C_{H} increases proportionally to the surface area
- R_{total} increases for KOH-etched
 - current concentrations on the peaks
 - more stable surface terminations (probably H)

Acknowledgements

- GenMik (Generation of Microstructures PhD Group)
- Ministry of Science, Research and Art of Baden-Württemberg, Germany

Thank you for your attention!